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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,938	12/12/2003	Lee W. Atkinson	200300687-1	1470

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EXAMINER	
PHAM, THOMAS K	
ART UNIT	**PAPER NUMBER**
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,938	ATKINSON ET AL.	
	Examiner	Art Unit	
	Thomas K. Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Notice to Applicants

1. Applicant's request for a pre-appeal brief conference in regard to the final Office action mailed on 12/04/2006 has been held. The finality of that action is withdrawn, PROSECUTION IS HEREBY REOPENED. A new ground of rejection set forth below.

Quotations of U.S. Code Title 35

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Rejections - 35 USC § 102

4. Claims 1-2, 4-5, 8-13 and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,526,253 ("Duley").

Regarding claim 1

Duley teaches the invention including a system, comprising: power management logic [see col. 5 lines 44-45]; an electrical load coupled to the power management logic and configurable to operate in accordance with any of a plurality of power states [see col. 5 lines 44-55]; wherein, if an operating voltage for the system is between two thresholds, the power management logic forces the electrical load to operate in a reduced power state [see col. 8 lines 48-54 and col. 8 lines 41-44, *if the output voltage is at a regulated range (thresholds), power is forced to operate at standby state*].

Regarding claim 12

Duley teaches the invention including a system, comprising: an electrical load configurable to operate in accordance with any of a plurality of power states [see col. 5 lines 44-55]; and power management means coupled to the load for forcing the system to operate in a reduced power state when an operating voltage is between two voltage levels [see col. 8 lines 48-54 and col. 8 lines 41-44, *if the output voltage is at a regulated range (thresholds), power is forced to operate at standby state*].

Regarding claim 16

Duley teaches the invention including a power management logic unit configured to operate in a system, comprising: control logic that receives first and second signals, determines whether an operating voltage is between first and second reference voltages based on the first and second

signals [see col. 5 lines 44-55] and, if so, causes the system to operate in a non-programmable, reduced performance mode [see col. 8 lines 48-54 and col. 8 lines 41-44, *if the output voltage is at a regulated range (thresholds), power is forced to operate at standby state*].

Regarding claim 18

Duley teaches the invention including a method, comprising: comparing an operating voltage to a first reference voltage and to a second reference voltage [see col. 5 lines 10-15]; and when the operating voltage is between the two reference voltages, requiring a system to operate in a less than full performance mode [see col. 8 lines 48-54 and col. 8 lines 41-44, *if the output voltage is at a regulated range (thresholds), power is forced to operate at standby state*].

Regarding claim 2

Duley teaches a pair of comparators coupling the operating voltage to inputs of the power management logic, each comparator having a reference voltage different from each other [see col. 8 lines 52-65].

Regarding claim 4

Duley teaches the power management logic determines whether the operating voltage is between the reference voltages [see col. 8 lines 15-21].

Regarding claim 5

Duley teaches the system comprises a computer [see col. 1 lines 35-40].

Regarding claim 8

Duley teaches if the power management logic determines the operating voltage is above both of the two thresholds, the power management logic permits the system to operate in a full performance power state [see col. 6 lines 29-36].

Regarding claim 9

Duley teaches if the power management logic determines the operating voltage is above both of the two thresholds, the power management logic permits the system to operate in any one of a plurality of power states [see col. 5 lines 10-21].

Regarding claim 10

Duley teaches the power states are programmable [see col. 8 lines 41-65].

Regarding claim 11

Duley teaches if the power management logic determines the operating voltage is below both of the two thresholds, the power management logic causes the system to operate in any one of a plurality of power states [see col. 5 lines 10-21].

Regarding claim 13

Duley teaches means for permitting the system to operate in any of a plurality of power states when the operating voltage is not between the two voltage levels [see col. 5 lines 44-55].

Regarding claim 15

Duley teaches means for determining whether the operating voltage is between the two voltage levels [see col. 8 lines 15-21].

Regarding claim 17

Duley teaches the control logic determines whether the operating voltage is not between the first and second reference voltages and, if so, permits the system to operate in a mode that requires more power than the reduced performance mode [see col. 5 lines 10-21].

Regarding claims 19 and 20

Duley the reference voltages comprise a first reference voltage and a second reference voltage and the first reference voltage is higher than the second reference voltage [see col. 4 lines 47-59], and the method further comprises permitting the system to operate in any one of a plurality of programmable modes only if the operating voltage is above the first reference voltage or below the second reference voltage [see col. 6 lines 29-36].

Claim Rejections - 35 USC § 103

5. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duley.

Regarding claim 3

Duley discloses an example of range anywhere from 5 volts to 20 volts (see col. 4 lines 50-57). *It should be noted that the threshold values set forth (e.g. 15.5 VDC and 14.5 VDC) is given very little patentable weight. In the absence of any new or unexpected results, the threshold values are considered to be set to any values operate on a specific device.*

6. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duley in view of U.S. Patent No. 6,967,522 ("Chandrakasan").

Regarding claim 6

Duley does not specifically teach the electrical load comprises a CPU coupled to the power management logic and the reduced power state comprises a reduced average clock frequency of a CPU clock.

However, Chandrakasan teaches the electrical load comprises a CPU coupled to the power management logic and the reduced power state comprises a reduced average clock frequency of a CPU clock [see FIG. 2 and Col. 8 lines 8-12].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the method of reducing CPU clock for managing power of Chandrakasan with the teaching of Duley because it would provide for the purpose of improving power efficiency of an electronic device.

Regarding claim 14

Duley does not specifically teach the means for forcing the system to operate in the reduced power state comprises means for reducing a clock frequency associated with a CPU in the system.

However, Chandrakasan teaches the means for forcing the system to operate in the reduced power state comprises means for reducing a clock frequency associated with a CPU in the system [see col. 9 lines 16-27].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the method of reducing CPU clock for managing power of Chandrakasan with the teaching of Duley because it would provide for the purpose of improving power efficiency of an electronic device.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Duley in view of U.S. Patent No. 5,991,883 ("Atkinson").

Regarding claim 7

Duley does not specifically teach the electrical load comprises a display and the reduced power state comprises a dimmed display.

However, Atkinson teaches a system for power conservation in a portable computer system including a dimmed LCD display (see Col. 2 lines 55-63) for the purpose of reducing the power of the display when high performance is not required (see Col. 2 lines 64-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the display system of Atkinson with the system of Duley for the purpose of reducing the power of the display when high performance is not required.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (571) 272-3689, Monday - Friday from 7:30 AM - 4:00 PM EST or contact Supervisor *Mr. Anthony Knight* at (571) 272-3687.

Any response to this office action should be mailed to: **Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.** Responses may also be faxed to the **official fax number (571) 273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas Pham
Primary Examiner

May 30, 2007